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09/652,495	08/31/2000	Salman Akram	3847US (98-541)	3659

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/652,495	Applicant(s) Akram
	Examiner Nitin Parekh	Art Unit 2811

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 6, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-3, 5-41, and 43-55* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-3, 5-41, and 43-55* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Jul 16, 2002* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Request for continued examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination (RCE) under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) is timely paid, the finality of the previous office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01-06-03 has been entered. An action on the RCE follows.

2. An amendment filed on 12-09-02 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US Pat. 6004867) in view of Lin (US Pat. 5258648).

Regarding claim 1, Kim et al disclose a chip scale package (CSP)/flip chip carrier (FCC) comprising:

- a semiconductor device/silicon chip (110 in Fig. 2) including an active surface having bond pads (112 in Fig. 2), the device being invertedly disposed on a first surface of a substrate (120 in Fig. 2)

- the substrate comprising a semiconductor material such as silicon (Col. 3, line 51) having substantially the same coefficient of thermal expansion (CTE) as that of the device/chip, the substrate having conductive traces (122 in Fig. 2) on the first surface, being disposed adjacent the active surface of the device and the substrate including a plurality of electrically conductive vias extending partially therethrough, the vias filled with an electrically conductive material (123 in Fig. 2; Col. 4, line 15), the vias having one end being in communication with/bonded to the conductive traces/contact areas and corresponding bond pads (122 and 112 respectively in Fig. 2) of the device

- an intermediate/passivation layer (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate

- electrically conductive metal bumps (130 in Fig. 2) such as solder (Col. 4, line 27; Col. 6, line 60) protruding from an another surface/second surface, the another surface being opposite to the device and in communication with respective electrically conductive vias

(Fig. 1 and 2; Col. 2, line 62- Col. 4, line 40).

Kim et al further disclose:

- forming direct vertical/via connections between vertically separated trace/metal layers using through-holes extending through the substrate (not numerically referenced in Fig. 1-3; Col. 4, line 55) providing an alignment of the vias and respective bond pads, and

- forming traces (122 in Fig. 2) anywhere in the substrate (top/bottom, middle layer, etc.-see Fig. 2 and 3; Col. 3, line 55) and forming the vias and pads (124/123 in Fig. 2) at any desired position on the surface of the substrate with respect to the position of the chip pads (Col. 4, line 9-25).

Kim et al fail to specify at least one conductive trace in communication with at least one electrically conductive via, the trace being carried on the another surface which is opposite from the surface adjacent to the device.

Lin teaches using a semiconductor device package (Fig. 4) comprising a substrate/interposer (22 in Fig. 3-6) having a surface adjacent to a device/chip (12 in Fig. 3-6) and an opposite surface, the substrate having electrically conductive vias (24 in Fig. 3 and 4) extending therethrough (Col. 5, line 1-5) and solder balls/bumps (32 in Fig. 3, 4 and 6) connected at the ends of the vias. Lin further teaches the substrate having conductive traces in communication of the vias/solder balls at both ends, the

traces being carried on the opposite surface/bottom surface (Col. 8, line 55-60; 42/44 in Fig. 6; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one conductive trace in communication with at least one electrically conductive via, the trace being carried on a surface of the substrate which is opposite from the surface adjacent to the device as taught by Lin so that the desired routing for the vias and power/ground connections for the terminals/solder balls can be achieved in Kim et al's package.

Regarding claim 2, as explained above for claim 1, Kim et al disclose electrically conductive metal bumps (130 in Fig. 2) such as solder (Col. 4, line 27; Col. 6, line 60) protruding from the surface opposite to the one adjacent the device and the bumps being in communication with the electrically conductive vias (Fig. 1 and 2; Col. 2, line 62- Col. 4, line 40).

Regarding claim 3, as explained above for claim 1, Kim et al disclose electrically conductive vias extending substantially/directly through the substrate.

Regarding claim 5, as explained above for claim 1, Kim et al disclose the substrate of the semiconductor device and the substrate comprising the same type of semiconductor material such as silicon.

Regarding claim 6, as explained above for claim 1, Kim et al disclose the substrate of the device and the substrate comprising the semiconductor materials having substantially the same CTE.

Regarding claim 7, as explained above for claim 1, Kim et al disclose the substrate of the device comprising silicon.

Regarding claim 8, as explained above for claim 1, Kim et al disclose the semiconductor material comprising silicon.

Regarding claim 9, Kim et al disclose a first thickness of the semiconductor device/chip (110 in Fig. 2) being greater than that of the semiconductor substrate (120 in Fig. 2) but fail to specify those being substantially the same.

Lin teaches using the chip and the substrate (12 and 22 respectively in Fig. 1 and 3) having respective first and second thicknesses being substantially the same.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device and the substrate having substantially the same thickness as taught by Lin so that manufacturing yield and cycle time can be improved in Kim et al's package.

Regarding claim 10, Kim et al disclose a first thickness of the semiconductor device/chip (110 in Fig. 2) being greater than that of the semiconductor substrate (120 in Fig. 2).

Regarding claim 15, as explained above for claim 1, Kim et al further disclose the intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate adhering the device and the substrate and the conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 18, as explained above for claim 15, Kim et al disclose the electrically conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 19, as explained above for claim 1, Kim et al disclose the electrically conductive vias/conductive material being bonded/electrically connected to the corresponding bond pads.

Regarding claim 21, as explained above for claim 1, Kim et al disclose the device being invertedly disposed adjacent the substrate.

Regarding claim 22, as explained above for claim 1, Kim et al disclose the bond pads contacting the corresponding vias.

Regarding claim 26, as explained above for claim 15, Kim et al disclose using the intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate and the electrically conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 27, as explained above for claim 18, Kim et al disclose the electrically conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 28, as explained above for claim 15, Kim et al disclose using the intermediate/passivation layer adhering the device to the substrate.

Regarding claim 30, as explained above for claim 2, Kim et al disclose the conductive metal bumps protruding from the surface opposite to the one adjacent the device and the bumps being in communication with the electrically conductive vias.

Regarding claim 31, as explained above for claim 2, Kim et al disclose the conductive metal bumps being solder.

Regarding claim 32, as explained above for claim 1, Kim et al disclose the semiconductor device and the substrate comprising the same type of semiconductor material.

Regarding claim 33, as explained above for claim 1, Kim et al disclose the semiconductor device and the substrate comprising the same type of semiconductor material such as silicon.

Regarding claim 34, as explained above for claim 1, Kim et al disclose the substrate of the semiconductor device comprising silicon.

Regarding claim 35, Kim et al fail to specify those being substantially the same.

As explained above for claim 9, Lin teaches using the chip and the substrate (12 and 22 respectively in Fig. 1 and 3) having respective first and second thicknesses being substantially the same.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device and the substrate having substantially the same thickness as taught by Lin so that manufacturing yield and cycle time can be improved in Kim et al's package.

Regarding claim 36, as explained above for claim 1, Kim et al disclose the thickness of the semiconductor substrate being less than that of the semiconductor device/chip.

Regarding claim 43, Kim et al and Lin teach substantially the entire claimed structure as applied to claim 1 above including a CSP having a flip chip carrier (FCC) where a first end of the vias being positioned to substantially align with the corresponding bond pads of the chip and at least one conductive trace laterally extending from a second end of the via and being carried on the second/another surface which is opposite from the surface adjacent to the device.

Regarding claim 44, as explained above for claim 1, Kim et al teach the vias comprising the electrically conductive material.

Regarding claim 50, as explained above for claim 1, Kim et al teach the substrate comprising silicon.

Regarding claim 51, Kim et al fail to specify using a conductive bump adjacent an end of at least one of the conductive traces located opposite to the second end of at least one via.

As explained above for claim 1, Lin teaches using a semiconductor device package (Fig. 4) comprising a substrate/interposer (22 in Fig. 3-6) having a surface adjacent to a device/chip (12 in Fig. 3-6) and an opposite surface, the substrate having electrically conductive vias (24 in Fig. 3 and 4) extending therethrough (Col. 5, line 1-5) and solder balls/bumps (32 in Fig. 3, 4 and 6) connected at the ends of the vias. Lin further teaches the substrate having conductive traces in communication of the vias/solder balls at both ends, the traces being carried on the opposite surface/bottom surface (Col. 8, line 55-60; 42/44 in Fig. 6; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a conductive bump adjacent an end of at least one of the conductive traces located opposite to the second end of at least one via as taught by Lin so that the desired routing for the vias and power/ground connections for the terminals/solder balls can be achieved and the wiring resistance can be reduced in Kim et al's package.

Regarding claim 52, as explained above for claim 1, Kim et al disclose the bumps comprising solder.

5. Claims 11-14, 20, 23-25, 37-41 and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US Pat. 6004867) and Lin (US Pat. 5258648) as applied to claim 1 above, and further in view of Gnadinger (US Pat. 5229647).

Regarding claim 11, Kim et al and Lin teach substantially the entire claimed structure as applied to claim 1 above, but fail to specify the another surface of the substrate being partially coated with an insulating material.

Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer

extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the another surface of the substrate being partially coated with an insulating material as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 12, Kim et al and Lin fail to specify an insulative material comprising a layer extending substantially over the another surface of the substrate.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate having the insulating material extending substantially over the another surface as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 13, Kim et al and Lin fail to specify an insulative material comprising an oxide.

As explained above for claim 11, Gnadinger teaches using a wafer level packaging where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising an oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 14, Kim et al and Lin fail to specify an insulative material comprising a silicon oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that

having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising a silicon oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 20, as explained above for claim 1, Kim et al and Lin disclose a region comprising bond pad, via and respective material but fail to specify forming a diffusion region comprising a bond pad and via material.

Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region between the bond pad and via, the region securing the device to the substrate as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Kim et al's package.

Regarding claim 23, Kim et al and Lin disclose a region comprising bond pad, via and respective material but fail to specify forming a diffusion region comprising a bond pad via and respective material.

As explained above for claim 20, Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region comprising the bond pad and via as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Kim et al and Lin's package.

Regarding claim 24, Kim et al and Lin disclose a region comprising bond pad, via and respective material but fail to specify forming a diffusion region comprising a bond pad and via material.

As explained above for claim 20, Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region comprising the bond pad and via material as

taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Kim et al and Lin's package.

Regarding claim 25, Kim et al and Lin disclose a region comprising bond pad, via and respective material but fail to specify forming a diffusion region at least partially securing the device to the substrate.

As explained above for claim 20, Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region between the bond pad and via, the region securing the device to the substrate as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Kim et al's package.

Regarding claim 37, Kim et al and Lin fail to specify the another surface of the substrate comprising an insulating material.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide,

nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the another surface of the substrate comprising an insulating material as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 38, Kim et al and Lin fail to specify at least one of the conductive vias being exposed through the insulating material.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the vias being exposed through the insulating material as taught by Gnadinger so that the bonding strength and interconnect reliability can be improved in Kim et al's package.

Regarding claim 39, Kim et al and Lin fail to specify an insulative material comprising an oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising an oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 40, Kim et al and Lin fail to specify an insulative material comprising silicon oxide.

As explained above for claim 11, Gnadinger teaches using a wafer level packaging where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to

that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising silicon oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 41, Kim et al and Lin fail to specify an insulative material comprising a layer extending substantially over the another surface of the substrate.

As explained above for claim 12, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate having the insulating material extending substantially over the another surface as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 45, Kim et al and Lin fail to specify an insulating material being disposed on at least a portion of at least one surface of the substrate.

Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material being disposed on at least a portion of at least one surface of the substrate as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 46, Kim et al and Lin fail to specify the insulative material comprising an oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that

having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising an oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 47, Kim et al and Lin fail to specify an insulative material comprising a silicon oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising a silicon oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 48, Kim et al and Lin fail to specify an insulative material comprising a layer extending substantially over the another surface of the substrate.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate having the insulating material extending substantially over the another surface as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 49, Kim et al and Lin fail to specify the vias being exposed through the insulating material.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that

having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the vias being exposed through the insulating material as taught by Gnadinger so that the bonding strength and interconnect reliability can be improved in Kim et al's package.

6. Claims 16, 17, 29 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US Pat. 6004867) and Lin (US Pat. 5258648) as applied to claim 1 above,

Regarding claim 16, Kim et al and Lin teach substantially the entire claimed structure as applied to claim 1 above including an intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate but fail to specify using the intermediate layer comprising an adhesive material.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection and bonding/adhesion for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising an adhesive

material as taught by Higgins, III so that the passivation and surface protection can be improved in Kim et al's package.

Regarding claim 17, as explained above for claim 15, Kim et al and Lin disclose using an intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate but fail to specify using the intermediate layer comprising polyimide.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising polyimide as taught by Higgins, III so that the passivation and surface protection can be improved in Kim et al's package.

Regarding claim 29, Kim et al and Lin fail to specify using the intermediate layer comprising polyimide.

As explained above for claim 17, Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising polyimide as taught by Higgins, III so that the passivation and surface protection can be improved in Kim et al and Lin's package.

Regarding claim 53, as explained above for claim 15, Kim et al and Lin fail to specify using an adhesive layer disposed adjacent the first surface of the substrate.

As explained above for claim 15, Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide/solder mask, silicon oxide, nitride, etc. (Col. 2, line 65, Col. 3, line 25-40) on a first surface of the chip/substrate to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an adhesive layer disposed adjacent the first surface of the substrate as taught by Higgins, III so that the passivation and surface protection can be improved in Kim et al's package.

Regarding claim 54, Kim et al and Lin fail to specify the adhesive layer comprising polyimide.

As explained above for claim 15 Higgins, III teaches, Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide/solder

Response to Arguments

7. Applicant's arguments with respect to claims 1-3, 5-41 and 43-55 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

02-26-03

Tom Thomas

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